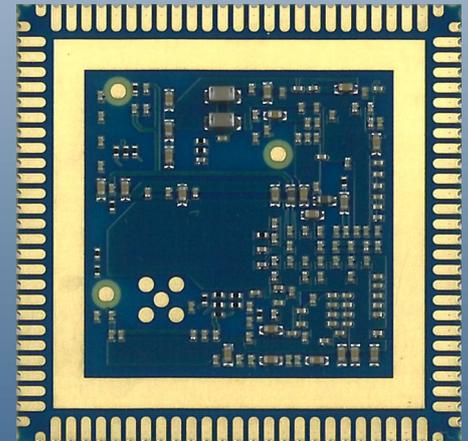## QS-Series - QFN Style Solder-Down Computer On Module

- QS type solder-down version
- 29mm square
- 4 mm total height
- QFN type lead style
  - 1mm pitch
  - 108 pads
- Visual solder joint inspection possible after soldering
- Defined return path for all signals
- 5V power supply

Key Features

- NXP i.MX 95   6x Cortex®-A55 up to 1.8 GHz
                        Cortex®-M7 up to 800 MHz
                        Cortex®-M33

- RAM   2 GB
- ROM   4 GB eMMC
- Grade   Industrial
- Temperature   -25°C to 85°C
- Display support

  - MIPI-DSI 4-lane (mux w/ MIPI-CSI)
  - Arm® Mali™ G310 3D GPU
    OpenGL® ES 3.2, Vulkan® 1.2, OpenCL™ 3.0
  - Enhanced, Separate 2D GPU
  - 4K60P H.264/H.265 encode or decode

- Vision and Machine Learning

  - 1x 4-lane CSI + 1x 4-lane CSI/DSI combo
  - 2 TOPS eIQ Neutron NPU
  - NXP ISP w/ RGB-IR, 500 mpx/sec

- Connectivity

  - 2x USB 2.0
  - 2x 1Gb Ethernet
  - 1x eMMC/SD, 2x CAN-FD
  - 1x PCIe® Gen 3
  - 3x UART, 3x I²C, 2x SPI, PWM, SAI
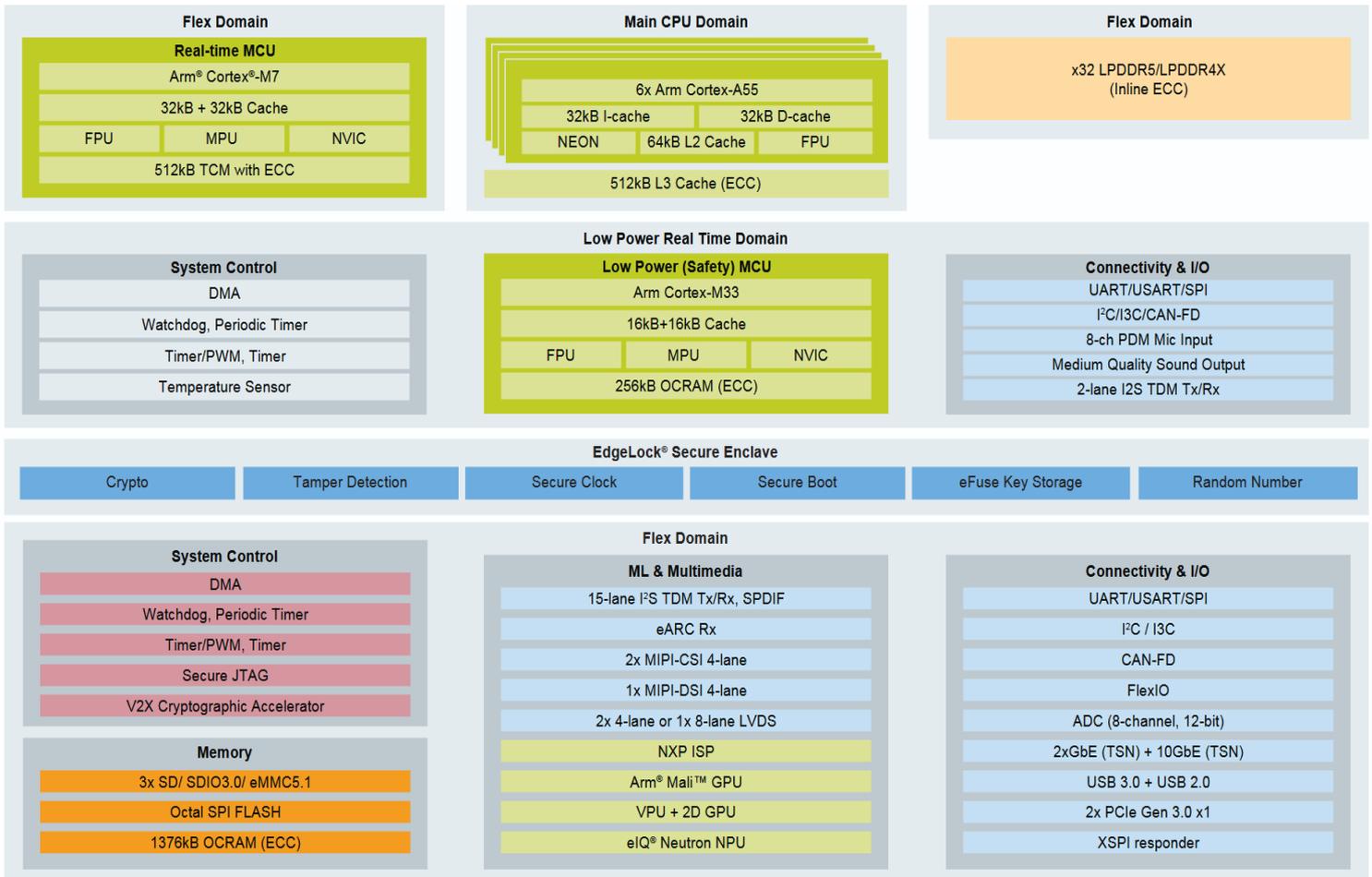 - Up to 60x 3.3V General Purpose I/O

OS Support
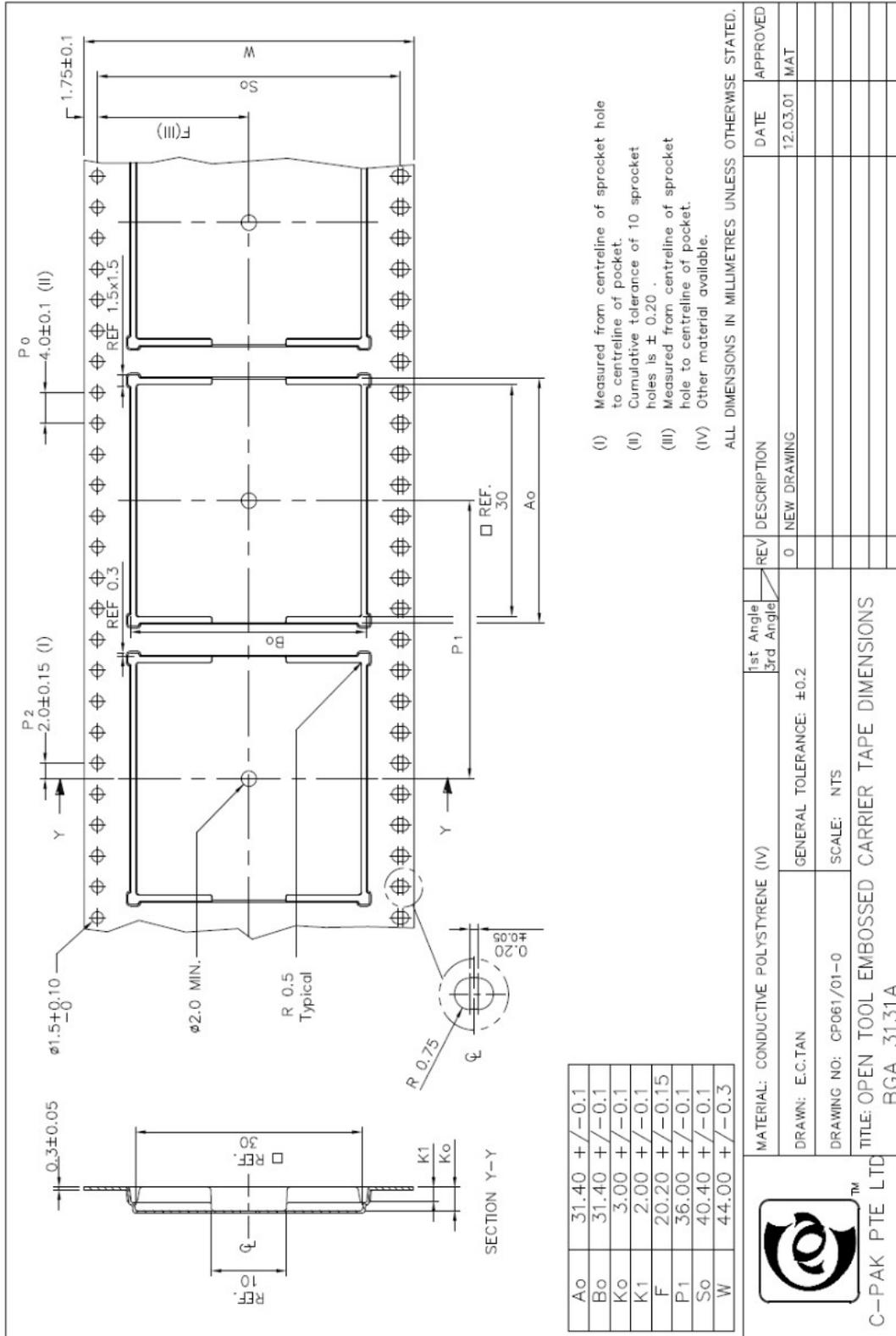
- Linux

i.MX 95

NXP

Flex Domain

Real-time MCU

Arm® Cortex®-M7

32kB + 32kB Cache

FPU	MPU	NVIC

512kB TCM with ECC

Main CPU Domain

6x Arm Cortex-A55	
32kB I-cache	32kB D-cache
NEON	64kB L2 Cache	FPU

512kB L3 Cache (ECC)

Flex Domain

x32 LPDDR5/LPDDR4X (Inline ECC)

System Control

DMA
Watchdog, Periodic Timer
Timer/PWM, Timer
Temperature Sensor

Low Power Real Time Domain

Low Power (Safety) MCU

Arm Cortex-M33

16kB+16kB Cache

FPU	MPU	NVIC

256kB OCRAM (ECC)

Connectivity & I/O

UART/USART/SPI
I²C/I3C/CAN-FD
8-ch PDM Mic Input
Medium Quality Sound Output
2-lane I2S TDM Tx/Rx

EdgeLock® Secure Enclave

Crypto	Tamper Detection	Secure Clock	Secure Boot	eFuse Key Storage	Random Number

System Control

DMA
Watchdog, Periodic Timer
Timer/PWM, Timer
Secure JTAG
V2X Cryptographic Accelerator

Flex Domain

ML & Multimedia

15-lane I²S TDM Tx/Rx, SPDIF
eARC Rx
2x MIPI-CSI 4-lane
1x MIPI-DSI 4-lane
2x 4-lane or 1x 8-lane LVDS
NXP ISP
Arm® Mali™ GPU
VPU + 2D GPU
eIQ® Neutron NPU

Connectivity & I/O

UART/USART/SPI
I²C / I3C
CAN-FD
FlexIO
ADC (8-channel, 12-bit)
2xGbE (TSN) + 10GbE (TSN)
USB 3.0 + USB 2.0
2x PCIe Gen 3.0 x1
XSPI responder

Memory

3x SD/ SDIO3.0/ eMMC5.1
Octal SPI FLASH
1376kB OCRAM (ECC)

QSXP – QS95 – Differentiated Features and Ordering Information

	QSXP - i.MX 8M Plus	**QS95** - i.MX 95
Primary Arm® Core	4x Cortex®-A53 1.6 GHz	6x Cortex®-A55 1.8 GHz
Secondary Arm® Core	Cortex®-M7 800 MHz	Cortex®-M7 800 MHz Cortex®-M33
RAM	2 GB	2 GB
ROM	8 GB eMMC	4 GB eMMC
3D GPU	GC7000UL (2 shaders, OpenGL ES 2.0/3.0/3.1 OpenCL 1.2, Vulkan)	Arm® Mali™ G310
2D GPU	GC520L	Enhanced 2D GPU
AI/ML/DSP	NN Accel 2.3 TOPS Hi-Fi4 DSP 800 MHz	2 TOPS eIQ Neutron NPU
Video Decode	1080p60 H.264, H.265	4K60P H.264, H.265
Connectivity	1Gb Ethernet	2x 1Gb Ethernet

2026-03-02

QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It`s not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QS95 uses a ground loop on the bottom side. With this a defined ground connection is available for all signals.

Contact Assignments

Package Information

Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

Packaging

Ao	31.40	+/-0.1
Bo	31.40	+/-0.1
Ko	3.00	+/-0.1
K1	2.00	+/-0.1
F	20.20	+/-0.15
P1	36.00	+/-0.1
So	40.40	+/-0.1
W	44.00	+/-0.3

MATERIAL: CONDUCTIVE POLYSTYRENE (IV)

DRAWN: E.C.TAN

DRAWING NO: CP061/01-0

TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS
BGA 3131A

GENERAL TOLERANCE: ±0.2

SCALE: NTS

1st Angle / 3rd Angle

REV	DESCRIPTION	DATE	APPROVED
0	NEW DRAWING	12.03.01	MAT

C-PAK PTE LTD

THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

SECTION Y-Y

Pinout

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
				Refer to i.MX 95 manuals for details!		
MIPI CSI						
1	PHY		MIPI_CSI1_D0_N			
2	PHY		MIPI_CSI1_D0_P			
3	PHY		MIPI_CSI1_D1_N			
4	PHY		MIPI_CSI1_D1_P			
5	PHY		MIPI_CSI1_CLK_N			
6	PHY		MIPI_CSI1_CLK_P			
7	PHY		MIPI_CSI1_D2_N			
8	PHY		MIPI_CSI1_D2_P			
9	PHY		MIPI_CSI1_D3_N			
10	PHY		MIPI_CSI1_D3_P			
MIPI DSI/CSI						
11	PHY		MIPI_DSICSI1_D0_N			
12	PHY		MIPI_DSICSI1_D0_P			
13	PHY		MIPI_DSICSI1_D1_N			
14	PHY		MIPI_DSICSI1_D1_P			
15	PHY		MIPI_DSICSI1_CLK_N			
16	PHY		MIPI_DSICSI1_CLK_P			
17	PHY		MIPI_DSICSI1_D2_N			
18	PHY		MIPI_DSICSI1_D2_P			
19	PHY		MIPI_DSICSI1_D3_N			
20	PHY		MIPI_DSICSI1_D3_P			
CAN						
21	3V3	CANTX_A	GPIO_IO28	I2C3.SDA **CAN3.TX** FLEXIO1.FLEXIO[28]	GPIO2.IO[28]	
22	3V3	CANRX_A	GPIO_IO29	I2C3.SCL **CAN3.RX** FLEXIO1.FLEXIO[29]	GPIO2.IO[29]	
23	3V3	CANTX_B	GPIO_IO25	USDHC3.DATA1 **CAN2.TX** TPM4.CH3 DAP.TCLK_SWCLK SPI7.PCS1 FLEXIO1.FLEXIO[25]	GPIO2.IO[25]	
24	3V3	CANRX_B	GPIO_IO27	USDHC3.DATA3 **CAN2.RX** TPM6.CH3 DAP.TMS_SWDIO SPI5.PCS1 FLEXIO1.FLEXIO[27]	GPIO2.IO[27]	
MISC						
25	3V3	PCIE_CLKREQ_B	GPIO_IO32	**PCIE1.CLKREQ_B** UART6.TX SPI4.PCS2	GPIO5.IO[12]	

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
				Refer to i.MX 95 manuals for details!		

SPI #1

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
26	3V3	SPI_SCK_A	GPIO_IO11	**SPI3.SCK** TPM5.EXTCLK UART7.RTS_B I2C8.SCL FLEXIO1.FLEXIO[11]	GPIO2.IO[11]	
27	3V3	SPI_MISO_A	GPIO_IO09	**SPI3.SIN** TPM3.EXTCLK UART7.RX I2C7.SCL FLEXIO1.FLEXIO[9]	GPIO2.IO[9]	
28	3V3	SPI_MOSI_A	GPIO_IO10	**SPI3.SOUT** TPM4.EXTCLK UART7.CTS_B I2C8.SDA FLEXIO1.FLEXIO[10]	GPIO2.IO[10]	
29	3V3	SPI_NSS_A	GPIO_IO08	**SPI3.PCS0** TPM6.CH0 UART7.TX I2C7.SDA FLEXIO1.FLEXIO[8]	GPIO2.IO[8]	

I2C

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
30	3V3	I2C_SCL_A	GPIO_IO03	**I2C4.SCL** SPI6.SCK UART5.RTS_B I2C6.SCL FLEXIO1.FLEXIO[3]	GPIO2.IO[3]	
31	3V3	I2C_SDA_A	GPIO_IO02	**I2C4.SDA** SPI6.SOUT UART5.CTS_B I2C6.SDA FLEXIO1.FLEXIO[2]	GPIO2.IO[2]	
32	3V3	I2C_SCL_B	GPIO_IO01	**I2C3.SCL** SPI6.SIN UART5.RX I2C5.SCL FLEXIO1.FLEXIO[1]	GPIO2.IO[1]	
33	3V3	I2C_SDA_B	GPIO_IO00	**I2C3.SDA** SPI6.PCS0 UART5.TX I2C5.SDA FLEXIO1.FLEXIO[0]	GPIO2.IO[0]	
34	3V3	I2C_SCL_C	I2C2_SCL	**I2C2.SCL** I3C1.PUR UART2.DCD_B TPM2.CH2 SAI1.RX_SYNC I3C1.PUR_B	GPIO1.IO[2]	
35	3V3	I2C_SDA_C	I2C2_SDA	**I2C2.SDA** UART2.RIN_B TPM2.CH3 SAI1.RX_BCLK	GPIO1.IO[3]	

SAI

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
36	3V3	SAI_RXD0	SAI1_RXD0	**SAI1.RX_DATA[0]** SAI1.MCLK SPI1.SOUT UART2.DSR_B MQS1.RIGHT	GPIO1.IO[14]	
37	3V3	SAI_TXD0	SAI1_TXD0	**SAI1.TX_DATA[0]** UART2.RTS_B SPI1.SCK UART1.DTR_B CAN1.TX CCMSRCGPCMIX.BOOT_MODE[3]	GPIO1.IO[13]	BOOT_MODE[3]
38	3V3	SAI_TXFS	SAI1_TXFS	**SAI1.TX_SYNC** SAI1.TX_DATA[1] SPI1.PCS0 UART2.DTR_B MQS1.LEFT CCMSRCGPCMIX.BOOT_MODE[2]	GPIO1.IO[11]	BOOT_MODE[2]
39	3V3	SAI_TXC	SAI1_TXC	**SAI1.TX_BCLK** UART2.CTS_B SPI1.SIN UART1.DSR_B CAN1.RX	GPIO1.IO[12]	

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
				Refer to i.MX 95 manuals for details!		

MISC

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
40	3V3	GPIO_A	GPIO_IO23	USDHC3.CMD SPDIF1.OUT CAN5.RX TPM6.CH1 I2C5.SCL FLEXIO1.FLEXIO[23]	GPIO2.IO[23]	
41	3V3	GPIO_B	GPIO_IO24	USDHC3.DATA0 TPM3.CH3 DAP.TDO_TRACESWO SPI6.PCS1 FLEXIO1.FLEXIO[24]	GPIO2.IO[24]	
42	POW	VDD_SD2_3V3				

USB

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
43	PHY	USBH_VBUS	USB2_VBUS			4K7 / 10K Voltage Divider
44	PHY	USBH_DN	USB2_D_N			
45	PHY	USBH_DP	USB2_D_P			
46	PHY	USBOTG_VBUS	USB1_VBUS			4K7 / 10K Voltage Divider
47	PHY	USBOTG_DN	USB1_D_N			
48	PHY	USBOTG_DP	USB1_D_P			

POWER SUPPLY & RESET

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
49	POW	VIN				
50						
51	3V3	POR_B				10K Pullup
52	3V3	BOOT_MODE				

ETHERNET #2

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
53	3V3	RGMII_TX_CTL RMII_TX_EN	ENET2_TX_CTL	NETC.ETH1_RGMII_TX_CTL UART4.DTR_B SAI2.TX_SYNC NETC.ETH1_RMII_TX_EN FLEXIO2.FLEXIO[20]	GPIO4.IO[20]	
54	3V3	RGMII_TX_CLK	ENET2_TXC	NETC.ETH1_RGMII_TX_CLK CCMSRCGPCMIX.ENET_REF_CLK_ROOT SAI2.TX_B CLKFLEXIO2.FLEXIO[21]	GPIO4.IO[21]	
55	3V3	RGMII_TXD3	ENET2_TD3	NETC.ETH1_RGMII_TXD[3] SAI2.RX_DATA[0] FLEXIO2.FLEXIO[16]	GPIO4.IO[16]	
56	3V3	RGMII_TXD2 RMII_REF50_CLK	ENET2_TD2	NETC.ETH1_RGMII_TXD[2] NETC.ETH1_RMII_REF50_CLK CCMSRCGPCMIX.ENET_REF_CLK_ROOT SAI2.RX_DATA[1] SAI4.TX_SYNC FLEXIO2.FLEXIO[17]	GPIO4.IO[17]	
57	3V3	RGMII_TXD1 RMII_TXD1	ENET2_TD1	NETC.ETH1_RGMII_TXD[1] UART4.RTS_B SAI2.RX_DATA[2] SAI4.TX_BCLK FLEXIO2.FLEXIO[18] NETC.ETH1_RMII_TXD[1]	GPIO4.IO[18]	
58	3V3	RGMII_TXD0 RMII_TXD0	ENET2_TD0	NETC.ETH1_RGMII_TXD[0] UART4.TX SAI2.RX_DATA[3] SAI4.TX_DATA[0] FLEXIO2.FLEXIO[19] NETC.ETH1_RMII_TXD[0]	GPIO4.IO[19]	
59	3V3	RGMII_RX_CLK RMII_RX_ER	ENET2_RXC	NETC.ETH1_RGMII_RX_CLK NETC.ETH1_RMII_RX_ER SAI2.TX_DATA[1] SAI4.RX_SYNC FLEXIO2.FLEXIO[23]	GPIO4.IO[23]	
60	3V3	RGMII_RX_CTL RMII_CRS_DV	ENET2_RX_CTL	NETC.ETH1_RGMII_RX_CTL UART4.DSR_B SAI2.TX_DATA[0] FLEXIO2.FLEXIO[22] NETC.ETH1_RMII_CRS_DV	GPIO4.IO[22]	

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
				Refer to i.MX 95 manuals for details!		
61	3V3	RGMII_RXD0 RMII_RXD0	ENET2_RD0	NETC.ETH1_RGMII_RXD[0] UART4.RX SAI2.TX_DATA[2] SAI4.RX_BCLK FLEXIO2.FLEXIO[24] NETC.ETH1_RMII_RXD[0]	GPIO4.IO[24]	
62	3V3	RGMII_RXD1 RMII_RXD1	ENET2_RD1	NETC.ETH1_RGMII_RXD[1] SPDIF1.IN SAI2.TX_DATA[3] SAI4.RX_DATA[0] FLEXIO2.FLEXIO[25] NETC.ETH1_RMII_RXD[1]	GPIO4.IO[25]	
63	3V3	RGMII_RXD2 RMII_RX_ER	ENET2_RD2	NETC.ETH1_RGMII_RXD[2] UART4.CTS_B SAI2.MCLK MQS2.RIGHT FLEXIO2.FLEXIO[26] NETC.ETH1_RMII_RX_ER	GPIO4.IO[26]	
64	3V3	RGMII_RXD3	ENET2_RD3	NETC.ETH1_RGMII_RXD[3] SPDIF1.OUT SPDIF1.IN MQS2.LEFT FLEXIO2.FLEXIO[27]	GPIO4.IO[27]	
65	3V3	MDIO	ENET2_MDIO	NETC.MDIO UART4.RIN_B SAI2.RX_B CLKFLEXIO2.FLEXIO[15]	GPIO4.IO[15]	
66	3V3	MDC	ENET2_MDC	NETC.MDC UART4.DCD_B SAI2.RX_SYNC FLEXIO2.FLEXIO[14]	GPIO4.IO[14]	
ETHERNET #1						
67		RGMII_RX_CLK RMII_RX_ER	ENET1_RXC	NETC.ETH0_RGMII_RX_CLK NETC.ETH0_RMII_RX_ER FLEXIO2.FLEXIO[9]	GPIO4.IO[9]	
68		RGMII_RX_CTL RMII_CRS_DV	ENET1_RX_CTL	NETC.ETH0_RGMII_RX_CTL UART3.DSR_B NETC.ETH0_RMII_CRS_DV USB2.OTG_PWR FLEXIO2.FLEXIO[8]	GPIO4.IO[8]	
69		RGMII_RXD0 RMII_RXD0	ENET1_RD0	NETC.ETH0_RGMII_RXD[0] UART3.RX NETC.ETH0_RMII_RXD[0] FLEXIO2.FLEXIO[10]	GPIO4.IO[10]	
70		RGMII_RXD1 RMII_RXD1	ENET1_RD1	NETC.ETH0_RGMII_RXD[1] UART3.CTS_B NETC.ETH0_RMII_RXD[1] LPTMR2.ALT0 FLEXIO2.FLEXIO[11]	GPIO4.IO[11]	
71		RGMII_RXD2 RMII_RX_ER	ENET1_RD2	NETC.ETH0_RGMII_RXD[2] NETC.ETH0_RMII_RX_ER LPTMR2.ALT1 FLEXIO2.FLEXIO[12]	GPIO4.IO[12]	
72		RGMII_RXD3	ENET1_RD3	NETC.ETH0_RGMII_RXD[3] LPTMR2.ALT2 FLEXIO2.FLEXIO[13]	GPIO4.IO[13]	
73		MDIO	ENET1_MDIO	NETC.MDIO UART3.RIN_B I3C2.SDA USB1.OTG_PWR FLEXIO2.FLEXIO[1]	GPIO4.IO[1]	
74		MDC	ENET1_MDC	NETC.MDC UART3.DCD_B I3C2.SCL FLEXIO2.FLEXIO[0]	GPIO4.IO[0]	
75		RGMII_TX_CLK	ENET1_TXC	NETC.ETH0_RGMII_TX_CLK CCMSRCGPCMIX.ENET_REF_CLK_ROOT FLEXIO2.FLEXIO[7]	GPIO4.IO[7]	
76		RGMII_TX_CTL RMII_TX_EN	ENET1_TX_CTL	NETC.ETH0_RGMII_TX_CTL UART3.DTR_B NETC.ETH0_RMII_TX_EN FLEXIO2.FLEXIO[6]	GPIO4.IO[6]	
77		RGMII_TXD3	ENET1_TD3	NETC.ETH0_RGMII_TXD[3] CAN2.TX USB2.OTG_ID FLEXIO2.FLEXIO[2]	GPIO4.IO[2]	

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
				Refer to i.MX 95 manuals for details!		
78		RGMII_TXD2 RMII_REF50_CLK	ENET1_TD2	NETC.ETH0_RGMII_TXD[2] NETC.ETH0_RMII_REF50_CLK CCMSRCGPCMIX.ENET_REF_CLK_ROOT CAN2.RX USB2.OTG_OC FLEXIO2.FLEXIO[3]	GPIO4.IO[3]	
79		RGMII_TXD1 RMII_TXD1	ENET1_TD1	NETC.ETH0_RGMII_TXD[1] UART3.RTS_B I3C2.PUR, I3C2.PUR_B USB1.OTG_OC FLEXIO2.FLEXIO[4] NETC.ETH0_RMII_TXD[1]	GPIO4.IO[4]	
80		RGMII_TXD0 RMII_TXD0	ENET1_TD0	NETC.ETH0_RGMII_TXD[0] UART3.TX NETC.ETH0_RMII_TXD[0] FLEXIO2.FLEXIO[5]	GPIO4.IO[5]	
SD						
81	POW	VDD_SDIO2				
82		SD_CD	SD2_CD_B	USDHC2.CD_B NETC.TMR_1588_TRIG1 I3C2.SCL FLEXIO1.FLEXIO[0]	GPIO3.IO[0]	
83		SD_D1	SD2_DATA1	USDHC2.DATA1 NETC.TMR_1588_CLK CAN2.RX FLEXIO1.FLEXIO[4]	GPIO3.IO[4]	
84		SD_D0	SD2_DATA0	USDHC2.DATA0 NETC.TMR_1588_PP2 CAN2.TX FLEXIO1.FLEXIO[3] CCMSRCGPCMIX.OBSERVE3	GPIO3.IO[3]	
85		SD_CLK	SD2_CLK	USDHC2.CLK NETC.TMR_1588_PP1 I3C2.SDA FLEXIO1.FLEXIO[1] CCMSRCGPCMIX.OBSERVE1	GPIO3.IO[1]	
86		SD_CMD	SD2_CMD	USDHC2.CMD NETC.TMR_1588_TRIG2 I3C2.PUR, I3C2.PUR_B FLEXIO1.FLEXIO[2] CCMSRCGPCMIX.OBSERVE2	GPIO3.IO[2]	
87		SD_D3	SD2_DATA3	USDHC2.DATA3 LPTMR2.ALT0 MQS2.LEFT NETC.TMR_1588_ALARM1 FLEXIO1.FLEXIO[6]	GPIO3.IO[6]	
88		SD_D2	SD2_DATA2	USDHC2.DATA2 NETC.TMR_1588_PP3 MQS2.RIGHT FLEXIO1.FLEXIO[5]	GPIO3.IO[5]	
UART						
89	3V3	UART_RXD_A	UART1_RXD	UART1.RX SECO.RX SPI2.SIN TPM1.CH0	GPIO1.IO[4]	
90	3V3	UART_TXD_A	UART1_TXD	UART1.TX SECO.TX SPI2.PCS0 TPM1.CH1 CCMSRCGPCMIX.BOOT_MODE[0]	GPIO1.IO[5]	BOOT_MODE[0]
91	3V3	UART_RXD_B	GPIO_IO05	TPM4.CH0 PDM.BIT_STREAM[0] CAN4.RX SPI7.SIN **UART6.RX** I2C6.SCL FLEXIO1.FLEXIO[5]	GPIO2.IO[5]	
92	3V3	UART_TXD_B	GPIO_IO04	TPM3.CH0 PDM.CLK CAN4.TX SPI7.PCS0 **UART6.TX** I2C6.SDA FLEXIO1.FLEXIO[4]	GPIO2.IO[4]	

PIN	TYPE	FUNCTION	i.MX95 Pad Name	Alternate functions	GPIO	Description
				Refer to i.MX 95 manuals for details!		
93	3V3	UART_RXD_C	GPIO_IO15	**UART3.RX** SPI8.SCK UART8.RTS_B UART4.RX FLEXIO1.FLEXIO[15]	GPIO2.IO[15]	
94	3V3	UART_TXD_C	GPIO_IO14	**UART3.TX** SPI8.SOUT UART8.CTS_B UART4.TX FLEXIO1.FLEXIO[14]	GPIO2.IO[14]	
95	3V3	UART_RTS_C	GPIO_IO17	SAI3.MCLK **UART3.RTS_B** SPI4.PCS1 UART4.RTS_B FLEXIO1.FLEXIO[17]	GPIO2.IO[17]	
96	3V3	UART_CTS_C	GPIO_IO16	SAI3.TX_BCLK PDM.BIT_STREAM[2] **UART3.CTS_B** SPI4.PCS2 UART4.CTS_B FLEXIO1.FLEXIO[16]	GPIO2.IO[16]	
SPI #2						
97	3V3	SPI_NSS_B	GPIO_IO18	SAI3.RX_BCLK **SPI5.PCS0, SPI4.PCS0** TPM5.CH2 FLEXIO1.FLEXIO[18]	GPIO2.IO[18]	
98	3V3	SPI_MISO_B	GPIO_IO19	SAI3.RX_SYNC PDM.BIT_STREAM[3] FLEXIO1.FLEXIO[19] **SPI5.SIN, SPI4.SIN** TPM6.CH2 SAI3.TX_DATA[0]	GPIO2.IO[19]	
99	3V3	SPI_MOSI_B	GPIO_IO20	SAI3.RX_DATA[0] PDM.BIT_STREAM[0] **SPI5.SOUT, SPI4.SOUT** TPM3.CH1 FLEXIO1.FLEXIO[20]	GPIO2.IO[20]	
100	3V3	SPI_SCK_B	GPIO_IO21	SAI3.TX_DATA[0] PDM.CLK FLEXIO1.FLEXIO[21] **SPI5.SCK, SPI4.SCK** TPM4.CH1 SAI3.RX_BCLK	GPIO2.IO[21]	

ADC						
50A	ANALOG		ADC_IN1			
51A	ANALOG		ADC_IN0			
PCIe						
25A	PHY		PCIE1_RX0_P			
26A	PHY		PCIE1_RX0_N			
75A	PHY		PCIE_REF_OUT_CLK_P			
76A	PHY		PCIE_REF_OUT_CLK_N			
100A	PHY		PCIE1_TX0_P			
1A	PHY		PCIE1_TX0_N			

Pins used for manufacturing and debugging – leave unconnected

PIN		PIN		PIN	
C1	JTAG_TDI			C3	JTAG_TCK
		B2	JTAG_TDO		
A1	NOT CONNECTED			A3	JTAG_TMS

Onboard peripherals wiring

USED FOR		i.MX95 Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!		
eMMC	CMD	SD1_CMD	USDHC1.CMDFLEXIO1.FLEXIO[9]	GPIO3.IO[9]	
	CLK	SD1_CLK	USDHC1.CLKFLEXIO1.FLEXIO[8]	GPIO3.IO[8]	
	DAT0	SD1_DATA0	USDHC1.DATA0FLEXIO1.FLEXIO[10]	GPIO3.IO[10]	
	DAT1	SD1_DATA1	USDHC1.DATA1FLEXIO1.FLEXIO[11]	GPIO3.IO[11]	
	DAT2	SD1_DATA2	USDHC1.DATA2FLEXIO1.FLEXIO[12] CCMSRCGPCMIX.PMIC_READY	GPIO3.IO[12]	
	DAT3	SD1_DATA3	USDHC1.DATA3 FLEXSPI.A_SS1_B FLEXIO1.FLEXIO[13]	GPIO3.IO[13]	
	DAT4	SD1_DATA4	USDHC1.DATA4 FLEXSPI.A_DATA[4] FLEXIO1.FLEXIO[14] XSPI_SLV.DATA[4]	GPIO3.IO[14]	
	DAT5	SD1_DATA5	USDHC1.DATA5 FLEXSPI.A_DATA[5] USDHC1.RESET_B FLEXIO1.FLEXIO[15] XSPI_SLV.DATA[5]	GPIO3.IO[15]	
	DAT6	SD1_DATA6	USDHC1.DATA6 FLEXSPI.A_DATA[6] USDHC1.CD_B FLEXIO1.FLEXIO[16] XSPI_SLV.DATA[6]	GPIO3.IO[16]	
	DAT7	SD1_DATA7	USDHC1.DATA7 FLEXSPI.A_DATA[7] USDHC1.WP FLEXIO1.FLEXIO[17] XSPI_SLV.DATA[7]	GPIO3.IO[17]	
	DS	SD1_STROBE	USDHC1.STROBE FLEXSPI.A_DQS FLEXIO1.FLEXIO[18] XSPI_SLV.DQS	GPIO3.IO[18]	

Onboard peripherals wiring

USED FOR		i.MX95 Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!		
PMIC PF09	SDA	I2C1_SDA	I2C1.SDA, I3C1.SDA UART1.RIN_B TPM2.CH1 VPU.UART_TX	GPIO1.IO[1]	1K-PU
	SCL	I2C1_SCL	I2C1.SCL, I3C1.SCL UART1.DCD_B TPM2.CH0 VPU.UART_RX	GPIO1.IO[0]	10K-PU
	INTB	GPIO_IO34	UART6.CTS BSPI4.PCS0	GPIO5.IO[14]	10K-PU
	RSTB	POR_B			10K-PU VDD_BBSM_1V8
	PWRON	PMIC_ON_REQ			100K-PD
	STBY	PMIC_STBY_REQ			100K-PD
	FCCU0	FCCU_ERR0			
	FCCU1	WDOG_ANY & POR_B			
	GPIO1	SD2_VSELECT	USDHC2.VSELECT USDHC2.WP LPTMR2.ALT2 FLEXIO1.FLEXIO[19] CCMSRCGPCMIX.EXT_CLK1	GPIO3.IO[19]	
	GPIO2	SD2_RESET_B	USDHC2.RESET_B LPTMR2.ALT1 NETC.TMR_1588_GCLK FLEXIO1.FLEXIO[7]	GPIO3.IO[7]	10K-PU VDD_SDIO2
	GPIO3				PF53_SOC_EN
	GPIO4				PF53_ARM_EN
PMIC PF53_SOC	SDA	I2C1_SDA	I2C1.SDA, I3C1.SDA UART1.RIN_B TPM2.CH1 VPU.UART_TX	GPIO1.IO[1]	
	SCL	I2C1_SCL	I2C1.SCL, I3C1.SCL UART1.DCD_B TPM2.CH0 VPU.UART_RX	GPIO1.IO[0]	
	PWRON				PF53_SOC_EN
PMIC PF53_ARM	SDA	I2C1_SDA	I2C1.SDA, I3C1.SDA UART1.RIN_B TPM2.CH1 VPU.UART_TX	GPIO1.IO[1]	
	SCL	I2C1_SCL	I2C1.SCL, I3C1.SCL UART1.DCD_B TPM2.CH0 VPU.UART_RX	GPIO1.IO[0]	
	PWRON				PF53_ARM_EN